# DUAL LOW VOLTAGE H-BRIDGE IC

**Check for Samples: DRV8835**

## FEATURES

- **Dual-H-Bridge Motor Driver**
  - **Capable of Driving Two DC Motors or One Stepper Motor**
  - **Low MOSFET On-Resistance: HS + LS 305 mΩ**
- **1.5-A Maximum Drive Current Per H-Bridge**
- **Bridges May Be Paralleled for 3-A Drive Current**
- **Separate Motor and Logic Supply Pins:**
  - **0-V to 11-V Motor-Operating Supply-Voltage Range**
  - **2-V to 7-V Logic Supply-Voltage Range**
- **Separate Logic and Motor Power Supply Pins**
- **Flexible PWM or PHASE/ENABLE Interface**
- **Low-Power Sleep Mode With 95-nA Maximum Supply Current**
- **Tiny 2-mm x 3-mm WSON Package**

## APPLICATIONS

- **Battery-Powered:**
  - **Cameras**
  - **DSLR Lenses**
  - **Consumer Products**
  - **Toys**
  - **Robotics**
  - **Medical Devices**

## DESCRIPTION

The DRV8835 provides an integrated motor driver solution for cameras, consumer products, toys, and other low-voltage or battery-powered motion control applications. The device has two H-bridge drivers, and can drive two DC motors or one stepper motor, as well as other devices like solenoids. The output driver block for each consists of N-channel power MOSFET's configured as an H-bridge to drive the motor winding. An internal charge pump generates needed gate drive voltages.

The DRV8835 can supply up to 1.5-A of output current per H-bridge. It operates on a motor power supply voltage from 0 V to 11 V, and a device power supply voltage of 2 V to 7 V.

PHASE/ENABLE and IN/IN interfaces can be selected which are compatible with industry-standard devices.

Internal shutdown functions are provided for over current protection, short circuit protection, under voltage lockout and overtemperature.

The DRV8835 is packaged in a tiny 12-pin WSON package with PowerPAD™ (Eco-friendly: RoHS & no Sb/Br).

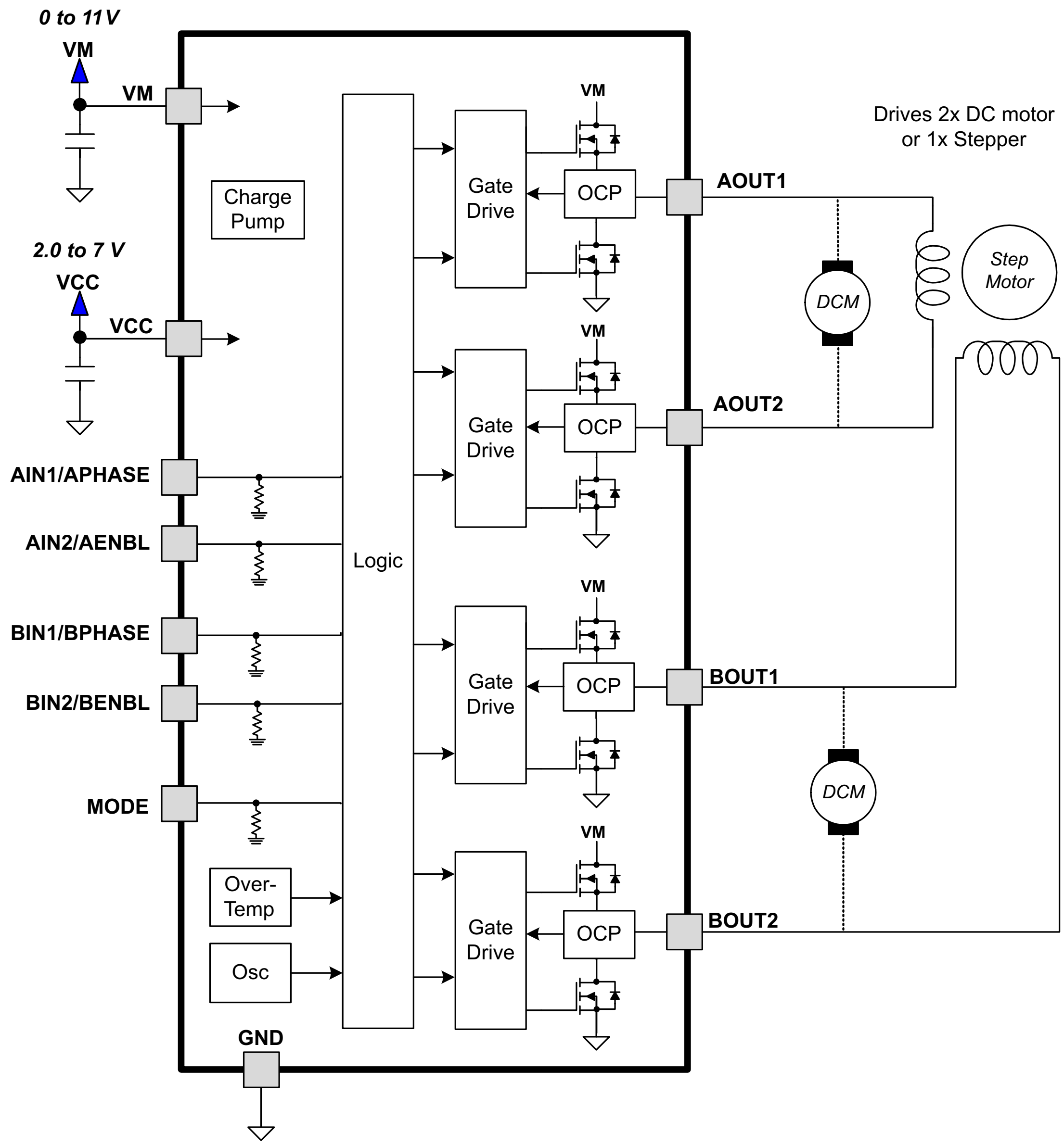
### ORDERING INFORMATION(1)

| PACKAGE(2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|
| PowerPAD™ (WSON) - DSS | Reel of 3000 | DRV8835DSSR | 835 |

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

# DEVICE INFORMATION

## Functional Block Diagram

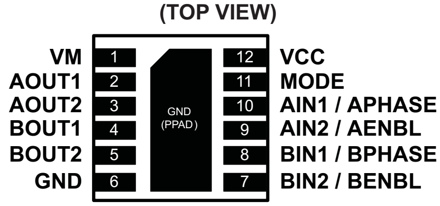


### Table 1. TERMINAL FUNCTIONS

| NAME | PIN | I/O(1) | DESCRIPTION | EXTERNAL COMPONENTS OR CONNECTIONS |
|---|---|---|---|---|
| **POWER AND GROUND** | | | | |
| GND | 6 | - | Device ground | |
| VM | 1 | - | Motor supply | Bypass to GND with a 0.1-μF (minimum) ceramic capacitor. |
| VCC | 12 | - | Device supply | Bypass to GND with a 0.1-μF (minimum) ceramic capacitor. |
| **CONTROL** | | | | |
| MODE | 11 | I | Input mode select | Logic low selects IN/IN mode.<br>Logic high selects PH/EN mode.<br>Internal pulldown resistor. |
| AIN1/APHASE | 10 | I | Bridge A input 1/PHASE input | IN/IN mode: Logic high sets AOUT1 high.<br>PH/EN mode: Sets direction of H-bridge A.<br>Internal pulldown resistor. |
| AIN2/AENBL | 9 | I | Bridge A input 2/ENABLE input | IN/IN mode: Logic high sets AOUT2 high.<br>PH/EN mode: Logic high enables H-bridge A.<br>Internal pulldown resistor. |
| BIN1/BPHASE | 8 | I | Bridge B input 1/PHASE input | IN/IN mode: Logic high sets BOUT1 high.<br>PH/EN mode: Sets direction of H-bridge B.<br>Internal pulldown resistor. |
| BIN2/BENBL | 7 | I | Bridge B input 2/ENABLE input | IN/IN mode: Logic high sets BOUT2 high.<br>PH/EN mode: Logic high enables H-bridge B.<br>Internal pulldown resistor. |
| **OUTPUT** | | | | |
| AOUT1 | 2 | O | Bridge A output 1 | Connect to motor winding A |
| AOUT2 | 3 | O | Bridge A output 2 | |
| BOUT1 | 4 | O | Bridge B output 1 | Connect to motor winding B |
| BOUT2 | 5 | O | Bridge B output 2 | |

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

**DSS PACKAGE**
**(TOP VIEW)**



## ABSOLUTE MAXIMUM RATINGS[1][2]

| | | VALUE | UNIT |
|---|---|---|---|
| VM | Power supply voltage range | –0.3 to 12 | V |
| VCC | Power supply voltage range | -0.3 to 7 | V |
| | Digital input pin voltage range | –0.5 to VCC + 0.5 | V |
| | Peak motor drive output current | Internally limited | A |
| | Continuous motor drive output current per H-bridge[3] | 1.5 | A |
| $T_J$ | Operating junction temperature range | –40 to 150 | °C |
| $T_{stg}$ | Storage temperature range | –60 to 150 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed.

## THERMAL INFORMATION

| THERMAL METRIC | | DRV8835 DSS 12 PINS | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance[1] | 50.4 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance[2] | 58 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance[3] | 19.9 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter[4] | 0.9 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter[5] | 20 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance[6] | 6.9 | |

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, $\psi_{JT}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, $\psi_{JB}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## RECOMMENDED OPERATING CONDITIONS

$T_A$ = 25°C (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Device power supply voltage range | 2 | | 7 | V |
| $V_M$ | Motor power supply voltage range | 0 | | 11 | V |
| $I_{OUT}$ | H-bridge output current[1] | 0 | | 1.5 | A |
| $f_{PWM}$ | Externally applied PWM frequency | 0 | | 250 | kHz |
| $V_{IN}$ | Logic level input voltage | 0 | | $V_{CC}$ | V |

(1) Power dissipation and thermal limits must be observed.

## ELECTRICAL CHARACTERISTICS

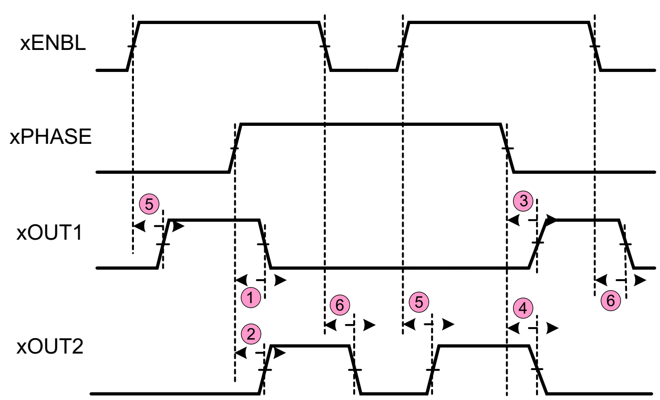
$T_A$ = 25°C, $V_M$ = 5 V, $V_{CC}$ = 3 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| $I_{VM}$ | VM operating supply current | No PWM, no load | | 85 | 200 | μA |
| | | 50 kHz PWM, no load | | 650 | 2000 | μA |
| $I_{VMQ}$ | VM sleep mode supply current | $V_M$ = 2 V, $V_{CC}$ = 0 V, all inputs 0 V | | 5 | | nA |
| | | $V_M$ = 5 V, $V_{CC}$ = 0 V, all inputs 0 V | | 10 | 95 | |
| $I_{VCC}$ | VCC operating supply current | | | 450 | 2000 | μA |
| $V_{UVLO}$ | VCC undervoltage lockout voltage | $V_{CC}$ rising | | | 2 | V |
| | | $V_{CC}$ falling | | | 1.9 | |
| **LOGIC-LEVEL INPUTS** | | | | | | |
| $V_{IL}$ | Input low voltage | | | | 0.3 x $V_{CC}$ | V |
| $V_{IH}$ | Input high voltage | | 0.5 x $V_{CC}$ | | | V |
| $I_{IL}$ | Input low current | $V_{IN}$ = 0 | -5 | | 5 | μA |
| $I_{IH}$ | Input high current | $V_{IN}$ = 3.3 V | | | 50 | μA |
| $R_{PD}$ | Pulldown resistance | | | 100 | | kΩ |
| **H-BRIDGE FETS** | | | | | | |
| $R_{DS(ON)}$ | HS + LS FET on resistance | $V_{CC}$ = 3 V, $V_M$ = 3 V, $I_O$ = 800 mA, $T_J$ = 25°C | | 370 | 420 | mΩ |
| | | $V_{CC}$ = 5 V, $V_M$ = 5 V, $I_O$ = 800 mA, $T_J$ = 25°C | | 305 | 355 | |
| $I_{OFF}$ | Off-state leakage current | | | | ±200 | nA |
| **PROTECTION CIRCUITS** | | | | | | |
| $I_{OCP}$ | Overcurrent protection trip level | | 1.6 | | 3.5 | A |
| $t_{DEG}$ | Overcurrent deglitch time | | | 1 | | μs |
| $t_{OCR}$ | Overcurrent protection retry time | | | 1 | | ms |
| $t_{DEAD}$ | Output dead time | | | 100 | | ns |
| $t_{TSD}$ | Thermal shutdown temperature | Die temperature | 150 | 160 | 180 | °C |

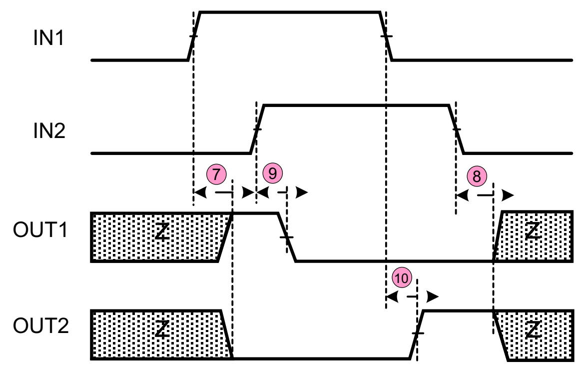
## TIMING REQUIREMENTS

$T_A = 25°C$, $V_M = 5$ V, $V_{CC} = 3$ V, $R_L = 20\ \Omega$

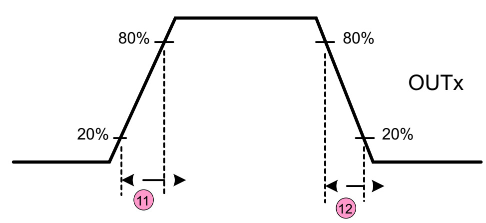
| NO. | PARAMETER | CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_1$ | Delay time, xPHASE high to xOUT1 low | | 300 | ns |
| 2 | $t_2$ | Delay time, xPHASE high to xOUT2 high | | 200 | ns |
| 3 | $t_3$ | Delay time, xPHASE low to xOUT1 high | | 200 | ns |
| 4 | $t_4$ | Delay time, xPHASE low to xOUT2 low | | 300 | ns |
| 5 | $t_5$ | Delay time, xENBL high to xOUTx high | | 200 | ns |
| 6 | $t_6$ | Delay time, xENBL high to xOUTx low | | 300 | ns |
| 7 | $t_7$ | Output enable time | | 300 | ns |
| 8 | $t_8$ | Output disable time | | 300 | ns |
| 9 | $t_9$ | Delay time, xINx high to xOUTx high | | 160 | ns |
| 10 | $t_{10}$ | Delay time, xINx low to xOUTx low | | 160 | ns |
| 11 | $t_R$ | Output rise time | 30 | 188 | ns |
| 12 | $t_F$ | Output fall time | 30 | 188 | ns |



PHASE/ENBL mode



IN/IN mode



# FUNCTIONAL DESCRIPTION

## Bridge Control

Two control modes are available in the DRV8835: IN/IN mode, and PHASE/ENABLE mode. IN/IN mode is selected if the MODE pin is driven low or left unconnected; PHASE/ENABLE mode is selected if the MODE pin is driven to logic high. The following tables show the logic for these modes.

**Table 2. IN/IN MODE**

| MODE | xIN1 | xIN2 | xOUT1 | xOUT2 | FUNCTION (DC MOTOR) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | Z | Z | Coast |
| 0 | 0 | 1 | L | H | Reverse |
| 0 | 1 | 0 | H | L | Forward |
| 0 | 1 | 1 | L | L | Brake |

**Table 3. PHASE/ENABLE MODE**

| MODE | xENABLE | xPHASE | xOUT1 | xOUT2 | FUNCTION (DC MOTOR) |
|---|---|---|---|---|---|
| 1 | 0 | X | L | L | Brake |
| 1 | 1 | 1 | L | H | Reverse |
| 1 | 1 | 0 | H | L | Forward |

## Sleep Mode

If the VCC pin is brought to 0 volts, the DRV8835 will enter a low-power sleep mode. In this state all unnecessary internal circuitry is powered down. For minimum supply current, all inputs should be low (0 V) during sleep mode.

## Power Supplies and Input Pins

There is a weak pulldown resistor (approximately 100 kΩ) to ground on the input pins.

VCC and VM may be applied and removed in any order. When VCC is removed, the device will enter a low power state and draw very little current from VM. The input pins should be kept at 0 V during sleep mode to minimize current draw.

The VM voltage supply does not have any undervoltage lockout protection (UVLO), so as long as VCC > 1.8 V, the internal device logic will remain active. This means that the VM pin voltage may drop to 0 V, however, the load may not be sufficiently driven at low VM voltages.

## Protection Circuits

The DRV8835 is fully protected against undervoltage, overcurrent and overtemperature events.

### Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled. After approximately 1 ms, the bridge will be re-enabled automatically.

Overcurrent conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown.

### Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled . Once the die temperature has fallen to a safe level operation will automatically resume.

### Undervoltage Lockout (UVLO)

If at any time the voltage on the VCC pins falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and internal logic will be reset. Operation will resume when VCC rises above the UVLO threshold.

## APPLICATIONS INFORMATION

### Parallel Mode

The two H-bridges in the DRV8835 can be connected in parallel for double the current of a single H-bridge. The drawing below shows the connections.

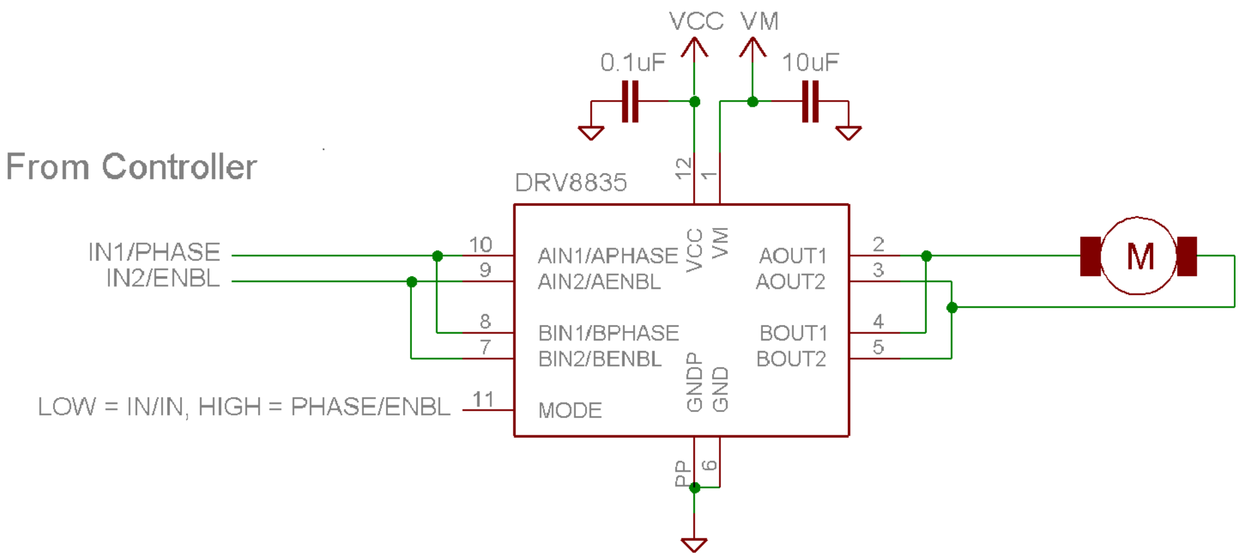



**Figure 1. Parallel Mode Connections**

# THERMAL INFORMATION

## Thermal Protection

The DRV8835 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

## Power Dissipation

Power dissipation in the DRV8835 is dominated by the power dissipated in the output FET resistance, or RDS(ON). Average power dissipation when running both H-bridges can be roughly estimated by:

$$P_{TOT} = 2 \times R_{DS(ON)} \times (I_{OUT(RMS)})^2 \quad (1)$$

Where $P_{TOT}$ is the total power dissipation, $R_{DS(ON)}$ is the resistance of the HS plus LS FETs, and $I_{OUT(RMS)}$ is the RMS output current being applied to each winding. $I_{OUT(RMS)}$ is equal to the approximately 0.7x the full-scale output current setting. The factor of 2 comes from the fact that there are two H-bridges.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

## Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report SLMA002, " PowerPAD™ Thermally Enhanced Package" and TI application brief SLMA004, " PowerPAD™ Made Easy", available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

## REVISION HISTORY

| Changes from Revision C (September 2013) to Revision D | Page |
|---|---|
| • Changed FEATURES bullet | 1 |
| • Changed motor supply voltage range in DESCRIPTION section | 1 |
| • Changed Motor power supply voltage range in RECOMMENDED OPERATING CONDITIONS | 4 |
| • Added $t_{OCR}$ and $t_{DEAD}$ parameters to ELECTRICAL CHARACTERISTICS | 5 |
| • Added paragraph to Power Supplies and Input Pins section | 7 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV8835DSSR | ACTIVE | WSON | DSS | 12 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 835 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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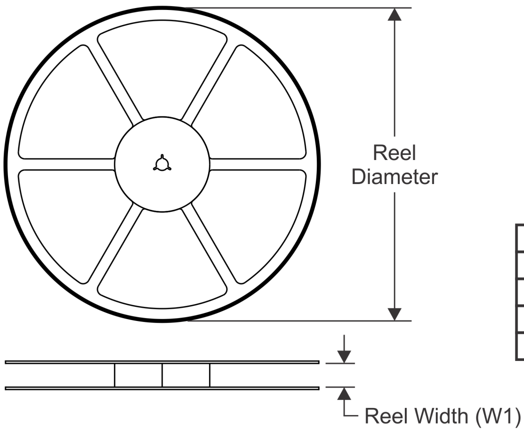
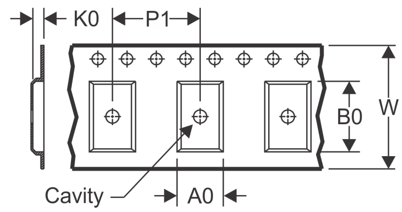
## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

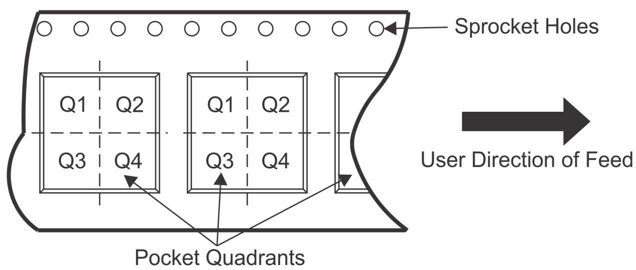



### TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

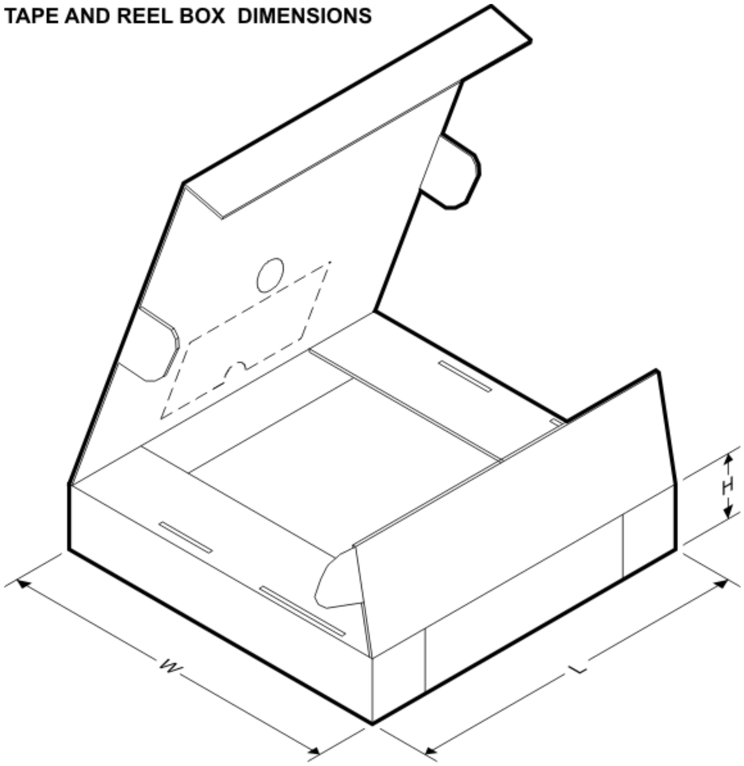
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV8835DSSR | WSON | DSS | 12 | 3000 | 180.0 | 8.4 | 2.25 | 3.25 | 1.05 | 4.0 | 8.0 | Q1 |

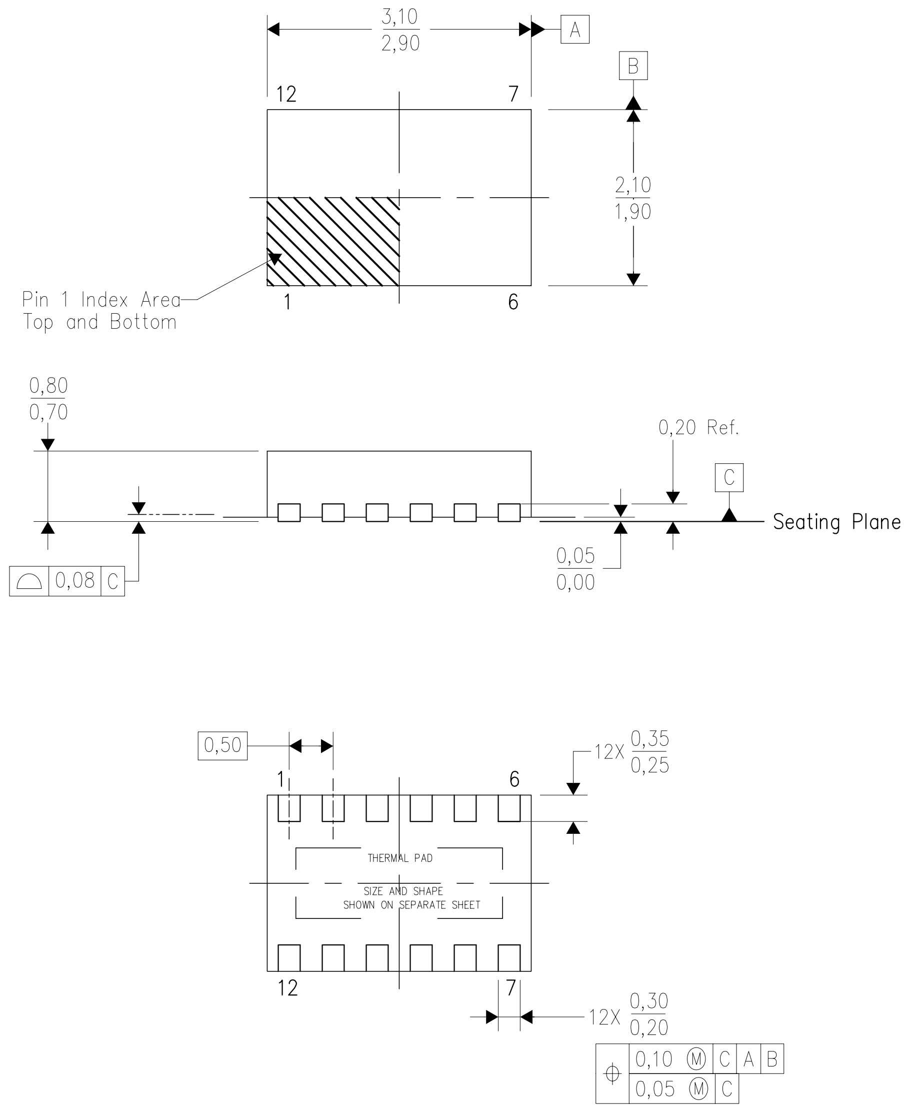
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DRV8835DSSR | WSON | DSS | 12 | 3000 | 210.0 | 185.0 | 35.0 |

DSS (R-PWSON-N12) PLASTIC SMALL OUTLINE NO-LEAD

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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. SON (Small Outline No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

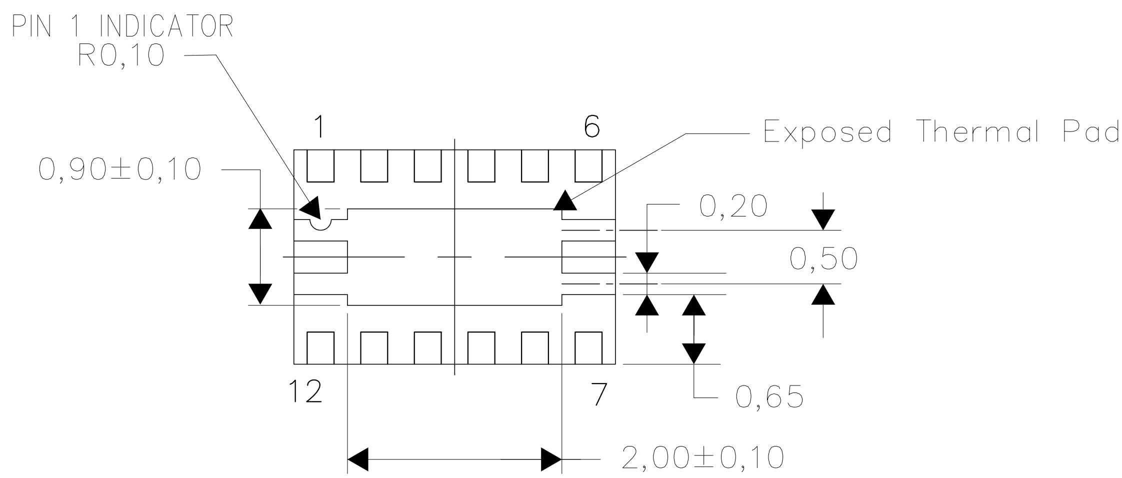
DSS (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Bottom View

Exposed Thermal Pad Dimensions

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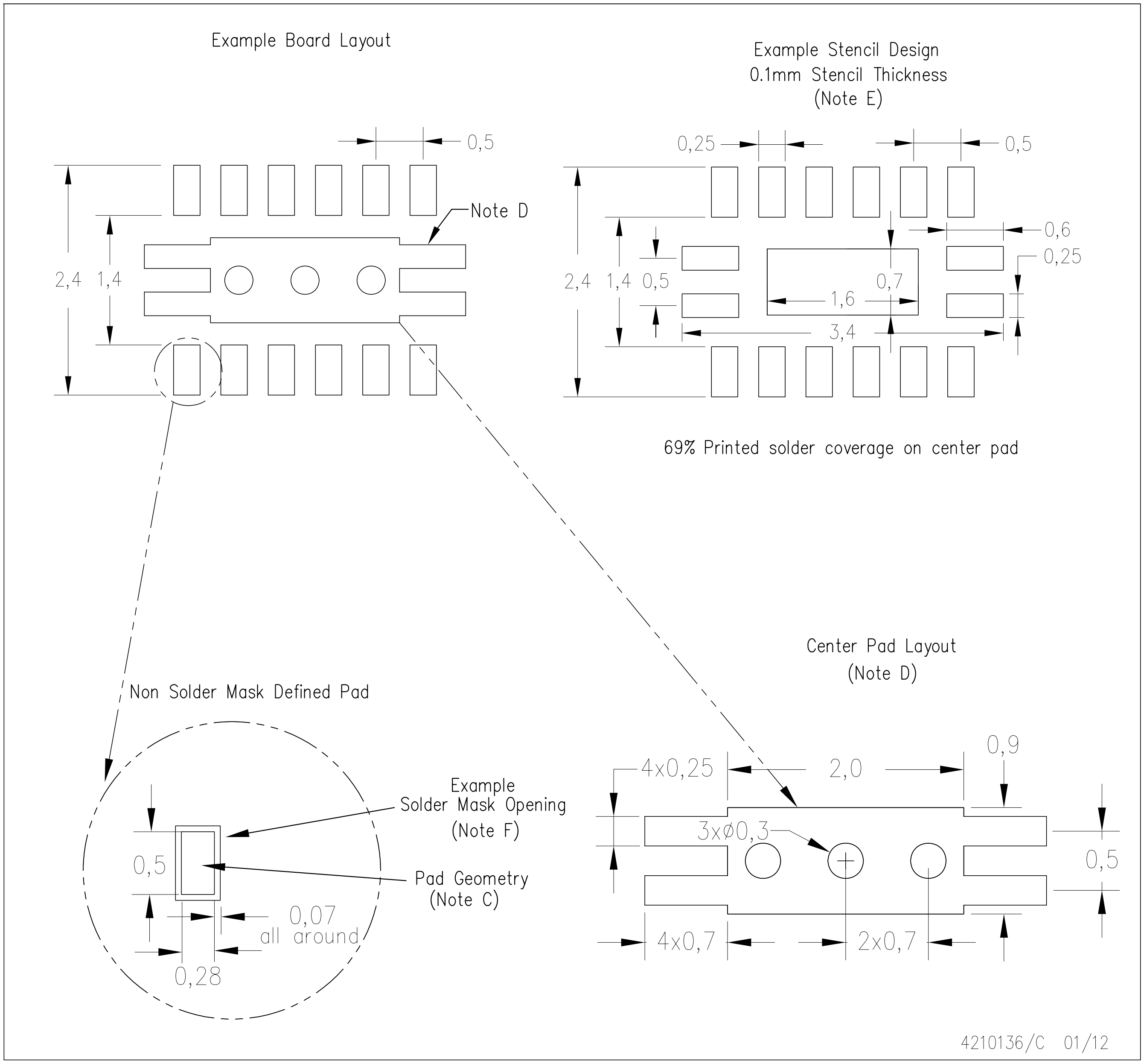
NOTE: All linear dimensions are in millimeters

DSS (R-PWSON-N12) PLASTIC SMALL OUTLINE NO-LEAD




NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

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