LPS25H

MEMS pressure sensor: 260-1260 hPa absolute digital output barometer

Datasheet - production data

HCLGA-10L
(2.5 x 2.5 x 1.0 mm)
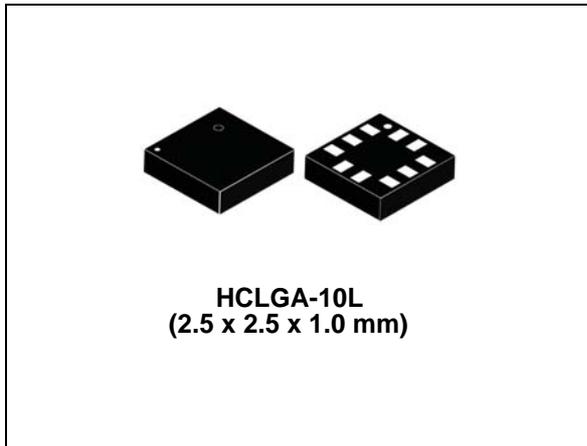
Features

- 260 to 1260 hPa absolute pressure range
- High-resolution mode: 1 Pa RMS
- Low power consumption:
  - Low resolution mode: 4 µA
  - High resolution mode: 25 µA
- High overpressure capability: 20x full scale
- Embedded temperature compensation
- Embedded 24-bit ADC
- Selectable ODR from 1 Hz to 25 Hz
- SPI and I²C interfaces
- Embedded FIFO
- Supply voltage: 1.7 to 3.6 V
- High shock survivability: 10,000 *g*
- Small and thin package
- ECOPACK® lead-free compliant

Applications

- Altimeter and barometer for portable devices
- GPS applications
- Weather Station Equipment
- Sport Watches

Description

The LPS25H is an ultra compact absolute piezoresistive pressure sensor. It includes a monolithic sensing element and an IC interface able to take the information from the sensing element and to provide a digital signal to the external world.

The sensing element consists of a suspended membrane realized inside a single mono-silicon substrate. It is capable to detect the absolute pressure and is manufactured with a dedicated process developed by ST.

The membrane is very small compared to the traditionally built silicon micromachined membranes. Membrane breakage is prevented by an intrinsic mechanical stopper.

The IC interface is manufactured using a standard CMOS process that allows a high level of integration to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LPS25H is available in a cavity holed LGA package (HCLGA). It is guaranteed to operate over a temperature range extending from -30 °C to +105 °C. The package is holed to allow external pressure to reach the sensing element.

Table 1. Device summary

Order codes	Temperature range [°C]	Package	Packing
LPS25HTR	-30 to +105	HCLGA-10L HCLGA-10L	Tape and reel
LPS25H			Tray

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Contents

1 Block diagram and pin description

Figure 1. LPS25H block diagram
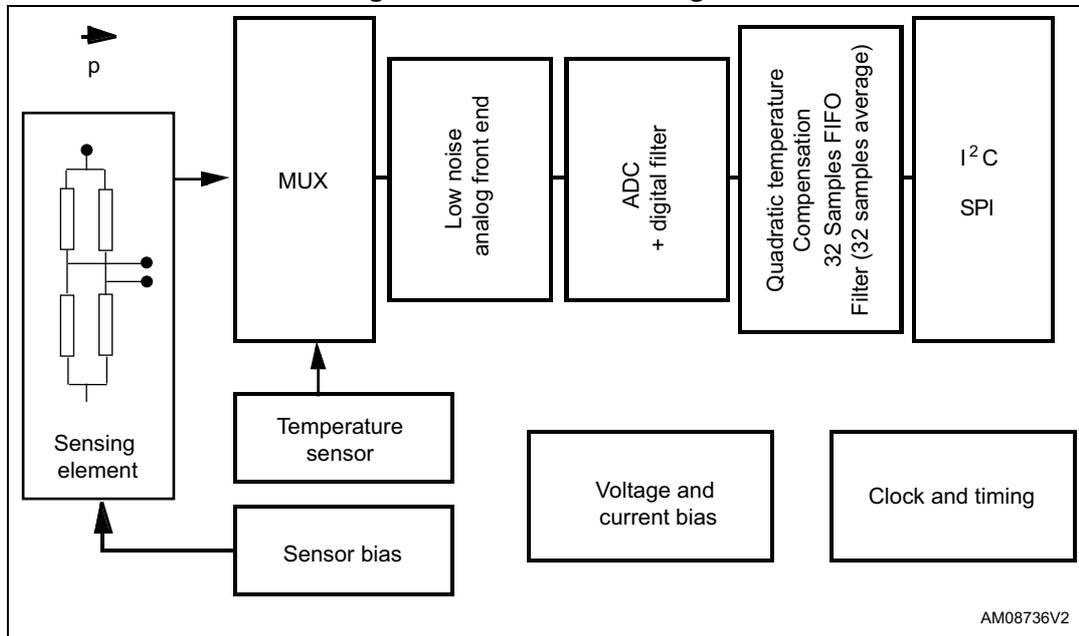
1.1 Pin description

Figure 2. Pin connection (bottom view)
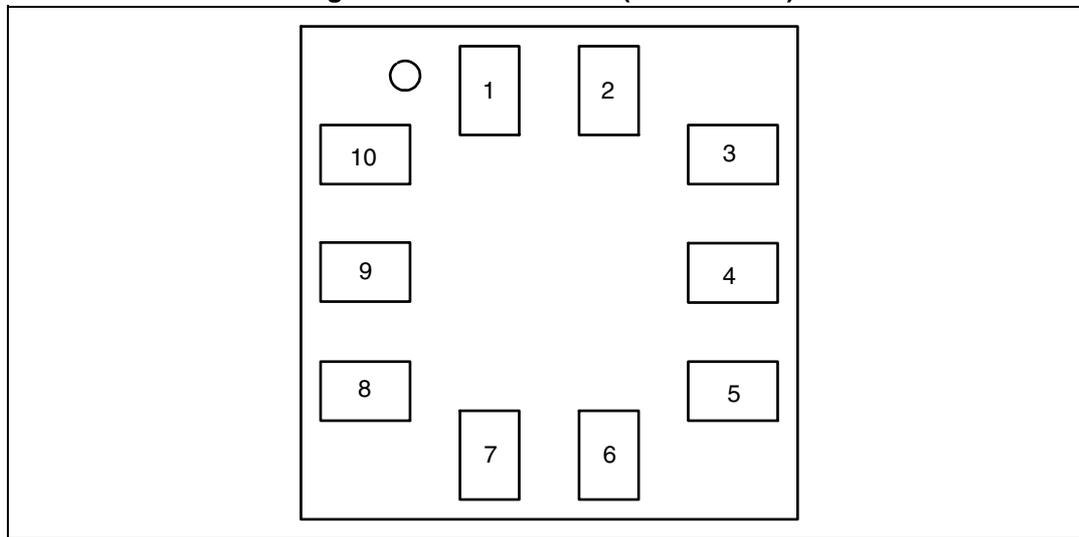
Table 2. Pin description

Pin n°	Name	Function
1	VDD_IO	Power supply for I/O pins
2	SCL SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
3	Reserved	Connect to GND
4	SDA SDI SDI/SDO	I²C serial data (SDA) 4-wire SPI serial data input (SDI) 3-wire serial data input /output (SDI/SDO)
5	SDO SA0	4-wire SPI serial data output (SDO) I²C less significant bit of the device address (SA0)
6	CS	SPI enable I²C/SPI mode selection (1: I²C mode; 0: SPI enabled)
7	INT1	Interrupt 1 (or data ready)
8	GND	0 V supply
9	GND	0 V supply
10	VDD	Power supply

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

V_{DD} = 2.5 V, T = 25 °C, unless otherwise noted.

Table 3. Mechanical characteristics

Symbol	Parameter	Test condition	Min.	Typ.[1]	Max.	Unit
Top	Operating temperature range		-30		105	°C
Tfull	Full accuracy temperature range		0		80	°C
Pop	Operating pressure range		260		1260	hPa
Pbits	Pressure output data			24		bits
Psens	Pressure sensitivity			4096		LSB/hPa
Paccrel	Relative accuracy over pressure[2]	P = 800 to 1100 hPa T = 25°C		± 0.1		hPa
PaccT	Absolute accuracy pressure over temperature[3]	P = 260 to 1260 hPa T = 20 ~ +60 °C		± 0.2		hPa
		P = 260 to 1260 hPa T = 0 ~ +80 °C		± 1		
Pnoise	Pressure noise[4]	without embedded filtering		0.03		hPa RMS
		with embedded filtering		0.01		
Tbits	Temperature output data			16		bits
Tsens	Temperature sensitivity			480		LSB/°C
Tacc	Absolute accuracy temperature	T= 0 ~ +65 °C		± 2		°C

1. Typical specifications are not guaranteed.

2. Characterization data. Parameter not tested at final test

3. Embedded quadratic compensation.

4. Pressure noise RMS evalueted in a controlled environment,based on the average standard deviation of 32 measurements at highest ODR.

2.2 Electrical characteristics

VDD = 2.5 V, T = 25 °C, unless otherwise noted.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.[1]	Max.	Unit
VDD	Supply voltage		1.7		3.6	V
VDD_IO	IO supply voltage		1.7		3.6	V
Idd	Supply current @ ODR 1 Hz, highest resolution			25		µA
IddPdn	Supply current in power-down mode T = 25 °C			0.5		µA

1. Typical specifications are not guaranteed.

2.3 Communication interface characteristics

2.3.1 SPI - serial peripheral interface

Subject to general operating conditions for Vdd and T_{OP}

Table 5. SPI slave timing values

Symbol	Parameter	Value [1]		Unit
		Min	**Max**	
tc(SPC)	SPI clock cycle	100		ns
fc(SPC)	SPI clock frequency		10	MHz
tsu(CS)	CS setup time	6		ns
th(CS)	CS hold time	8		
tsu(SI)	SDI input setup time	5		
th(SI)	SDI input hold time	15		
tv(SO)	SDO valid output time		50	
th(SO)	SDO output hold time	9		
tdis(SO)	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram
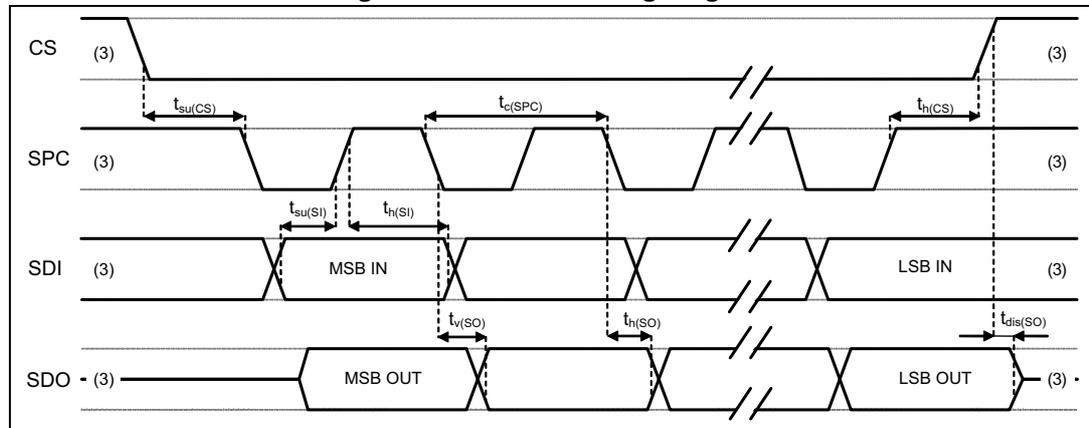
Note: Measurement points are done at 0.2· Vdd_IO and 0.8· Vdd_IO, for both port.

2.3.2 I²C - inter IC control interface

Subject to general operating conditions for Vdd and T_{OP}.

Table 6. I²C slave timing values

Symbol	Parameter [1]	I²C standard mode [1]		I²C fast mode [1]		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		μs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0	0.9	μs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$ [2]	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$ [2]	300	
$t_{h(ST)}$	START condition hold time	4		0.6		μs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I2C protocol requirement, not tested in production.

2. Cb = total capacitance of one bus line, in pF

Figure 4. I²C slave timing diagram
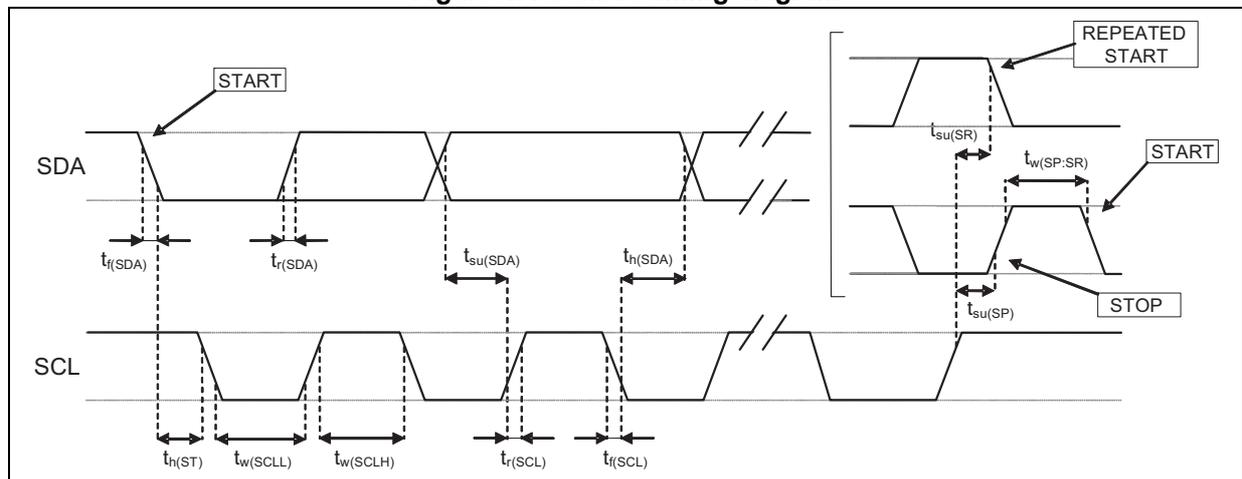
Note: *Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both port.*

2.4 Absolute maximum ratings

Stress above those listed as "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin	-0.3 to Vdd_IO +0.3	V
P	Overpressure	2	MPa
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: *Supply voltage on any pin should never exceed 4.8 V.*

This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part.

This is an ESD sensitive device, improper handling can cause permanent damage to the part.

3 Functionality

The LPS25H is a high resolution, digital output pressure sensor packaged in a HCLGA holed package. The complete device includes a sensing element based on a piezoresistive Wheatstone bridge approach, and an IC interface able to take the information from the sensing element to the external world, as a digital signal.

3.1 Sensing element

An ST proprietary process is used to obtain a mono-silicon μ-sized membrane for MEMS pressure sensors, without requiring substrate to substrate bonding. When pressure is applied, the membrane deflection induces an imbalance in the Wheatstone bridge piezoresistances, whose output signal is converted by the IC interface.

Intrinsic mechanical stoppers prevent breakage in case of pressure overstress, ensuring measurement repeatability.

The pressure inside the buried cavity under the membrane is constant and controlled by process parameters.

3.2 IC interface

The complete measurement chain is composed by a low-noise amplifier which converts the resistance unbalancing of the MEMS sensors (pressure and temperature) into an analog voltage that is finally available to the user by an analog-to-digital converter.

The pressure and temperature data may be accessed through an I²C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The LPS25H features a Data-Ready signal which indicates when a new set of measured pressure and temperature data are available thus simplifying data synchronization in the digital system that uses the device.

3.3 Factory calibration

The IC interface is factory calibrated at three temperatures and two pressures for sensitivity and accuracy.

The trimming values are stored inside the device by a non-volatile structure. Whenever the device is turned on, the trimming parameters are downloaded into the registers to be employed during normal operation. This allows the user to employ the device without requiring any further calibration.

3.4   FIFO

The LPS25H embeds FIFO register able to store 32 pressure output values, in order to improve the system power saving, since the host processor does not need to continuously poll data from the sensor, but it can wakeup only when requested and burst the significant data out from the FIFO.

The FIFO buffer is enabled by setting to 1 the FIFO_EN bit (21h - CTRL_REG2) and can work accordingly to 4 different modes: bypass mode, FIFO mode, Stream mode and FIFO Mean mode. Each mode is selected by the FIFO_MODE bits in FIFO_CTRL (2Eh).

Programmable Watermark level WTM_POINT4:0 (FIFO_CTRL register, 2Eh), EMPTY_FIFO or FULL_FIFO events can be enabled to generate dedicated interrupts on the INT1 pin (configuration through CTRL3 (22h) and CTRL4 (23h)).

3.4.1   Bypass mode (F_MODE2:0=”000” in FIFO_CTRL (2Eh))

The FIFO is not operational and for this reason it remains empty.

3.4.2   FIFO mode (F_MODE2:0=”001” in FIFO_CTRL (2Eh))

The data from PRESS_OUT_XL (28h), PRESS_OUT_L (29h) and PRESS_OUT_H (2Ah) are stored in the FIFO.

A Watermark interrupt can be enabled (WTM_EN bit in CTRL2 (21h) in order to be raised when the FIFO is filled to the level specified in the WTM_POINT4:0 bits of FIFO_CTRL (2Eh). The FIFO continues filling until it is full (32 slots of data for XL, L and H). When full, the FIFO stops collecting data from the input pressure data.

3.4.3   Stream mode (F_MODE2:0=”010” in FIFO_CTRL (2Eh))

The data from PRESS_OUT_XL (28h), PRESS_OUT_L (29h) and PRESS_OUT_H (2Ah) measurements are stored in the FIFO. The FIFO continues filling until it's full (32 slots of data for XL, L and H). When full, the FIFO discards the older data as the new arrive. A Watermark interrupt can be enabled and set as in FIFO mode.

Stream mode is use to implement the digital filter averaging the samples stored in the FIFO

3.4.4   FIFO mean mode (F_MODE2:0=”110” in FIFO_CTRL (2Eh))

The pressure data are not directly sent to the output register but are firstly stored in the FIFO to calculate the average. The FIFO Mean Mode can be enabled by setting the FIFO_MEAN_DEC bit (CTRL_REG2, 21h). The number of averaged samples can be set by changing the watermark in WTM_POINT4:0 bits of FIFO_CTRL (2Eh).

4   Application hints

Figure 5. LPS25H electrical connection
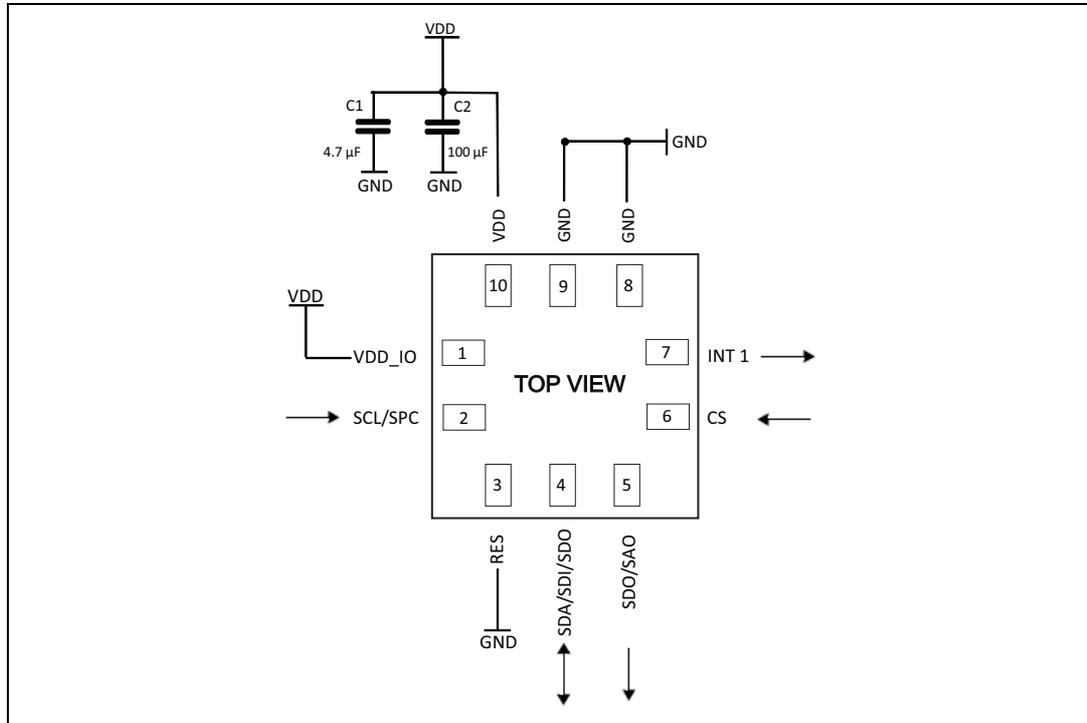
The device core is supplied through the VDD line. Power supply decoupling capacitors (100 nF, 4.7 µF) should be placed as near as possible to the supply pad of the device (common design practice).

The functionality of the device and the measured data outputs are selectable and accessible through the I²C/SPI interface. When using the I²C, CS must be tied high (i.e. connected to VDD_IO).

4.1   Soldering information

The HCLGA package is compliant with the ECOPACK® standard and it is qualified for soldering heat resistance according to JEDEC J-STD-020.

5   Digital interfaces

5.1   I²C serial interface

The registers embedded in the LPS25H may be accessed through both the I²C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I²C interface, CS line must be tied high (i.e. connected to Vdd_IO).

Table 8. Serial interface pin description

Pin name	Pin description
CS	SPI enable I²C/SPI mode selection (1: I²C mode; 0: SPI enabled)
SCL/SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDI/SDO	I²C serial data (SDA) 4-wire SPI serial data input (SDI) 3-wire serial data input /output (SDI/SDO)
SDO SAO	SPI serial data output (SDO) I²C less significant bit of the device address (SA0)

5.2   I²C serial interface (CS=High)

The LPS25H I²C is a bus slave. The I²C is employed to write data into registers whose content can also be read back.

The relevant I²C terminology is given in *Table 9*

Table 9. Serial interface pin description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bi-directional line used for sending and receiving the data to/from the interface. Both lines have to be connected to Vdd_IO through pull-up resistors.

The I²C interface is compliant with fast mode (400 kHz) I²C standards as well as with the normal mode.

5.2.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A start condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next data byte transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LPS25H is 101110xb. The **SDO**/**SA0** pad can be used to modify the less significant bit of the device address. If the SA0 pad is connected to voltage supply, LSb is '1' (address 1011101b), otherwise if the SA0 pad is connected to ground, the LSb value is '0' (address 1011100b). This solution permits to connect and address two different LPS25H devices to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded in the LPS25H behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, a 8-bit sub-address (SUB) will be transmitted: the 7 LSB represents the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is '1', the SUB (register address) will be automatically increased to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write) the master will transmit to the slave with direction unchanged. Table 10 explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

Table 10. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	101110	0	1	10111001 (B9h)
Write	101110	0	0	10111000 (B8h)
Read	101110	1	1	10111011 (BBh)
Write	101110	1	0	10111010 (BAh)

Table 11. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 12. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 13. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 14. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other functions, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real time function) the data line must be kept HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes incrementing the register address, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to be read.

In the presented communication format MAK is Master acknowledge and NMAK is no master acknowledge.

5.3 SPI bus interface

The LPS25H SPI is a bus slave. The SPI allows to write and read the registers of the device.

The serial interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 6. Read and write protocol
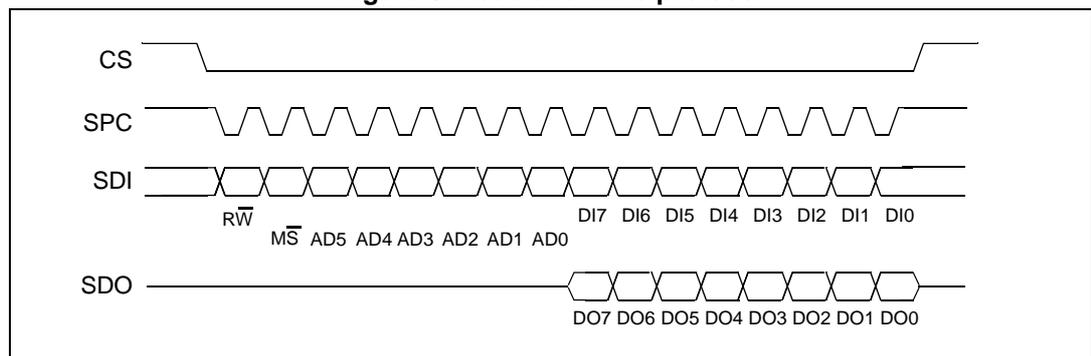
CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and returns to high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in the case of multiple bytes read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23,...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: RW̄ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip will drive **SDO** at the start of bit 8.

bit 1: MS̄ bit. When 0, the address will remain unchanged in multiple read/write commands. When 1, the address will be auto incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

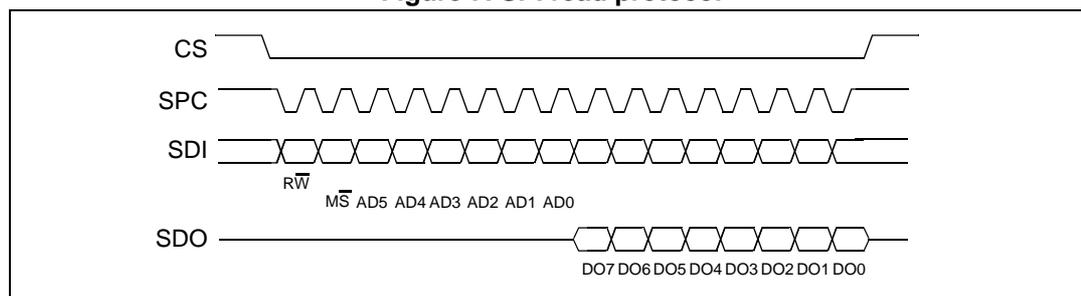*bit 8-15*: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods are added. When the MS̄ bit is 0 the address used to read/write data remains the same for every block. When MS̄ bit is 1 the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

5.3.1 SPI read

Figure 7. SPI read protocol

The SPI Read command is performed with 16 clock pulses. The multiple byte read command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: READ bit. The value is 1.

bit 1: MS̄ bit. When 0 do not increment address, when 1 increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

bit 16-...: data DO(...-8). Further data in multiple byte readings.

Figure 8. Multiple bytes SPI read protocol (2 bytes example)

5.3.2 SPI write

Figure 9. SPI write protocol

The SPI Write command is performed with 16 clock pulses. The multiple byte write command is performed adding blocks of 8 clock pulses at the previous one.
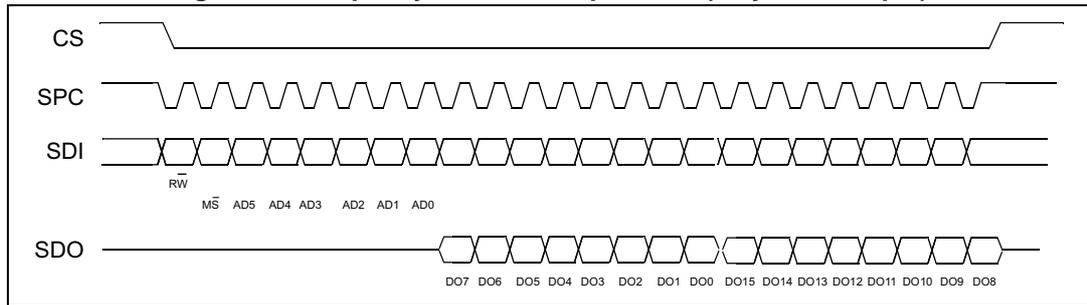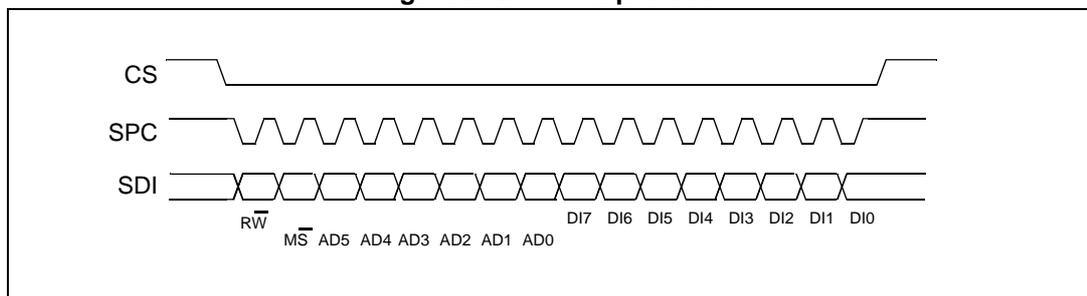
bit 0: WRITE bit. The value is 0.

bit 1: M$\overline{S}$ bit. When 0 do not increment the address, when 1 increment the address in multiple writings.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written in the device (MSb first).

bit 16-...: data DI(...-8). Further data in multiple byte writings.

Figure 10. Multiple bytes SPI write protocol (2 bytes example)

5.3.3 SPI read in 3-wires mode

A 3-wires mode is entered by setting to '1' bit SIM (SPI serial interface mode selection) in CTRL_REG1.

Figure 11. SPI read protocol in 3-wires mode
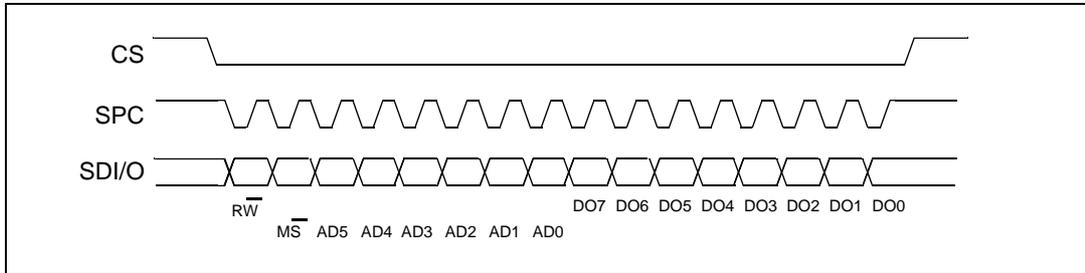
The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

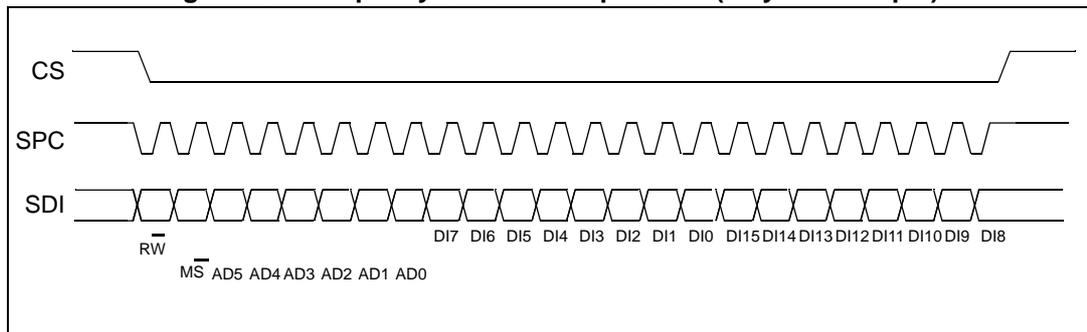**bit 1**: M$\overline{S}$ bit. When 0, do not increment the address, when 1, increment the address in multiple readings.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

Multiple read command is also available in 3-wires mode.

6 Register mapping

Table 15 provides a quick overview of the 8-bit registers embedded in the device.

Table 15. Registers address map

Name	Type	Register Address	Default	Function and comment
		Hex	Binary	
Reserved (Do not modify)		00-07 0D - 0E		Reserved
REF_P_XL	R/W	08	00000000	
REF_P_L	R/W	09	00000000	
REF_P_H	R/W	0A	00000000	
WHO_AM_I	R	0F	10111101	ID register
RES_CONF	R/W	10	00000101	
Reserved (Do not modify)		11-1F		Reserved
CTRL_REG1	R/W	20	00000000	
CTRL_REG2	R/W	21	00000000	
CTRL_REG3	R/W	22	00000000	
CTRL_REG4	R/W	23	00000000	
INT_CFG	R/W	24	00000000	
INT_SOURCE	R	25	00000000	
Reserved (Do not modify)		26		Reserved
STATUS_REG	R	27	00000000	
PRESS_POUT_XL	R	28	output	
PRESS_OUT_L	R	29	output	
PRESS_OUT_H	R	2A	output	
TEMP_OUT_L	R	2B	output	
TEMP_OUT_H	R	2C	output	
Reserved (Do not modify)		2D		Reserved
FIFO_CTRL	R/W	2E	00000000	
FIFO_STATUS	R	2F	00000000	
THS_P_L	R/W	30	00000000	
THS_P_H	R/W	31	00000000	
Reserved		32-38		
RPDS_L	R/W	39	00000000	
RPDS_H	R/W	3A	00000000	

Registers marked as *Reserved* must not be changed. The writing to those registers may cause permanent damages to the device.The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered-up.

7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve pressure and temperature data. The register address, made up of 7 bits, is used to identify them and to read/write the data through the serial interface.

7.1 REF_P_XL

Reference pressure (LSB data)

7	6	5	4	3	2	1	0
REFL7	REFL6	REFL5	REFL4	REFL3	REFL2	REFL1	REFL0

Address: 08h (R/W)

Reset: 00h

Description: The REF_P_XL register contains the lowest part of the reference pressure value that is sum to the sensor output pressure. The full reference pressure value is composed by REF_P_XL, REF_P_H & REF_P_L and is represented as 2's complement. The reference pressure value can also be used to detect a measured pressure beyond programmed limits (see INT_CFD at 23h), and for Autozero function (see RESET_AZ bit, at 20h).

[7:0] REFL7-0: LSB reference pressure data

7.2 REF_P_L

Reference pressure (middle part)

15	14	13	12	11	10	9	8
REFL15	REFL14	REFL13	REFL12	REFL11	REFL10	REFL9	REFL8

Address: 09h (R/W)

Reset: 00h

Description: The REF_P_L register contains the middle part of the reference pressure value that is sum to the sensor output pressure. (See REF_P_XL description).

[15:8] REFL15-8:Middle part reference pressure data

7.3 REF_P_H

Reference pressure (MSB data)

23	22	21	20	19	18	17	16
REFL23	REFL22	REFL21	REFL20	REFL19	REFL18	REFL17	REFL16

Address: 0Ah (R/W)

Reset: 00h

Description: The REF_P_H register contains the highest part of the reference pressure value that is sum to the sensor output pressure.(See description REF_P_XL).

[23:16] REFL23-16: MSB reference pressure data.

7.4 WHO_AM_I

Device identification

7	6	5	4	3	2	1	0
1	0	1	1	1	1	0	1

Address: 0Fh (R)

Description: Contains the device ID, **BDh**

7.5 RES_CONF

Pressure and temperature resolution mode

7	6	5	4	3	2	1	0
Reserved				AVGT1	AVGT0	AVGP1	AVGP0

Address: 10h (R/W)

Reset: 05h

Description: Pressure and Temperature internal average configuration.

[7:4] Reserved

[3:2] AVGP1-0: select the pressure internal average.See *Table 16*

[1:0] AVGT1-0: select the temperature internal average.See *Table 17*

Table 16. Pressure resolution configuration

AVGP1	AVGP0	Nr. internal average
0	0	8
0	1	32
1	0	128
1	1	512

Table 17. Temperature resolution configuration

AVGT1	AVGT0	Nr. internal average
0	0	8
0	1	16
1	0	32
1	1	64

7.6 CTRL_REG1

Control register 1

7	6	5	4	3	2	1	0
PD	ODR2	ODR1	ODR0	DIFF_EN	BDU	RESET_AZ	SIM

Address: 20h (R/W)

Reset: 00h

Description: Control register.

[7] PD: power down control.
Default value: 0
(0: power-down mode; 1: active mode)

[6:4] ODR2, ODR1, ODR0: output data rate selection.
Default value: 00
(see *Table 18*)

[3] DIFF_EN: Interrupt circuit enable.
Default value: 0
(0: interrupt generation disabled; 1: interrupt circuit enabled)

[2] BDU: block data update.
Default value: 0
(0: continuous update; 1: output registers not updated until MSB and LSB reading)

[1] RESET_AZ: Reset AutoZero function. Reset REF_P reg, set pressure to default value in RPDS register (@0x39/A)
(1: Reset. 0: disable)

[0] SIM: SPI Serial Interface Mode selection.
Default value: 0
(0: 4-wire interface; 1: 3-wire interface)

PD bit allows to turn on the device. The device is in power-down mode when PD = '0' (default value after boot). The device is active when PD is set to '1'.

ODR2- ODR1 - ODR0 bits allow to change the output data rates of pressure and temperature samples. The default value is "000" which corresponds to "one shot configuration" for both pressure and temperature output. ODR2, ODR1 and ODR0 bits can be configured as described in *Table 18*.

Table 18. Output data rate bit configurations

ODR2	ODR1	ODR0	Pressure (Hz)	Temperature (Hz)
0	0	0	One shot	
0	0	1	1 Hz	1 Hz
0	1	0	7 Hz	7 Hz
0	1	1	12.5 Hz	12.5 Hz
1	0	0	25 Hz	25 Hz
1	0	1	Reserved	

Table 18. Output data rate bit configurations

ODR2	ODR1	ODR0	Pressure (Hz)	Temperature (Hz)
1	1	0	Reserved	
1	1	1	Reserved	

DIFF_EN bit is used to enable the circuitry for the computing of differential pressure output. In default mode (DIFF_EN='0') the circuitry is turned off. It is suggested to turn on the circuitry only after the configuration of REF_P_x and THS_P_x.

BDU bit is used to inhibit the output registers update between the reading of upper and lower register parts. In default mode (BDU = '0'), the lower and upper register parts are updated continuously. If it is not sure to read faster than output data rate, it is recommended to set BDU bit to '1'. In this way, after the reading of the lower (upper) register part, the content of that output registers is not updated until the upper (lower) part is read too. This feature avoids reading LSB and MSB related to different samples.

RESET_AZ bit is used to Reset AutoZero function. Reset REF_P reg (@0x08..0A) set pressure reference to default value RPDS reg (0x39/3A). RESET_AZ is self cleared. See AutoZero function.

SIM bit selects the SPI serial interface mode.

0: (default value) 4-wire SPI interface mode selected.

1: 3-wire SPI interface mode selected

7.7 CTRL_REG2

Control register 2

7	6	5	4	3	2	1	0
BOOT	FIFO_EN	WTM_EN	FIFO_MEAN_DEC	0	SWRESET	AUTO_ZERO	ONE_SHOT

Address: 21h (R/W)

Reset: 00h

Description: Control register.

[7] BOOT: Reboot memory content. Default value: 0
(0: normal mode; 1: reboot memory content) Self-clearing upon completion)

[6] FIFO_EN: FIFO Enable. Default value: 0
(0: disable; 1: enable)

[5] WTM_EN: Enable FIFO Watermark level use. Default value 0
(0: disable; 1: enable)

[4] FIFO_MEAN_DEC: Enable 1Hz ODR decimation
(0: disable; 1 enable)

[3] I²C enable
(0: I2C enable;1: SPI disable)

[2] Software reset. Default value: 0
(0: normal mode; 1: software reset) Self-clearing upon completion)

[1] Autozero enable. Default value: 0
(0: normal mode; 1: autozero enable)

[0] One shot enable. Default value: 0
(0: waiting for start of conversion; 1: start for a new dataset)

Description:

BOOT bit is used to refresh the content of the internal registers stored in the Flash memory block. At the device power-up the content of the Flash memory block is transferred to the internal registers related to trimming functions to permit a good behavior of the device itself. If for any reason, the content of the trimming registers is modified, it is sufficient to use this bit to restore the correct values. When BOOT bit is set to '1' the content of the internal Flash is copied inside the corresponding internal registers and is used to calibrate the device. These values are factory trimmed and they are different for every device. They permit good behavior of the device and normally they should not be changed. At the end of the boot process the BOOT bit is set again to '0' by hardware. BOOT bit takes effect after one ODR clock cycle.

SWRESET is the software reset bit. The device is reset to the power on configuration if the SWRESET bit is set to '1' and BOOT is set to '1'.

AUTO_ZERO, when set to '1', the actual pressure output is copied in the REF_P_H & REF_P_L & REF_P_XL and kept as reference and the PRESS_OUT_H & PRESS_OUT_L & PRESS _OUT_XL is the difference between this reference and the pressure sensor value.

ONE_SHOT bit is used to start a new conversion when ODR2..0 bits in CTRL_REG1 are set to "000". Write '1' in ONE_SHOT to trigger a single measurement of pressure and

temperature. Once the measurement is done, ONE_SHOT bit will self-clear and the new data are available in the output registers, and the STATUS_REG bits are updated.

7.8   CTRL_REG3

Interrupt control

7	6	5	4	3	2	1	0
INT_H_L	PP_OD	Reserved				INT1_S2	INT1_S1

Address: 22h (R/W)

Reset: 00h

Description: Control register.

   [7] INT_H_L: Interrupt active high, low. Default value: 0
        (0: active high; 1: active low)

   [6] PP_OD: Push-pull/open drain selection on interrupt pads. Default value: 0
        (0: push-pull; 1: open drain)

  [5:2] Reserved

  [1:0]   INT1_S2, INT1_S1: data signal on INT1 pad control bits. Default value: 00
   (see *Table 19*)

Table 19. Interrupt configurations

INT1_S2	INT1_S1	INT1 pin
0	0	Data signal (see CTRL_REG4)
0	1	Pressure high (P_high)
1	0	Pressure low (P_low)
1	1	Pressure low OR high

The device features one fully-programmable interrupt sources (*INT1*) that can be configured to trigger different pressure events. *Figure 12* shows the block diagram of the interrupt generation block and output pressure data.

The device may also be configured to generate, through interrupt pins, a Data Ready signal (*Drdy*) which indicates when a new measured pressure data is available, thus simplifying data synchronization in digital systems or to optimize the system power consumption.

Figure 12. Interrupt generation block and output pressure data
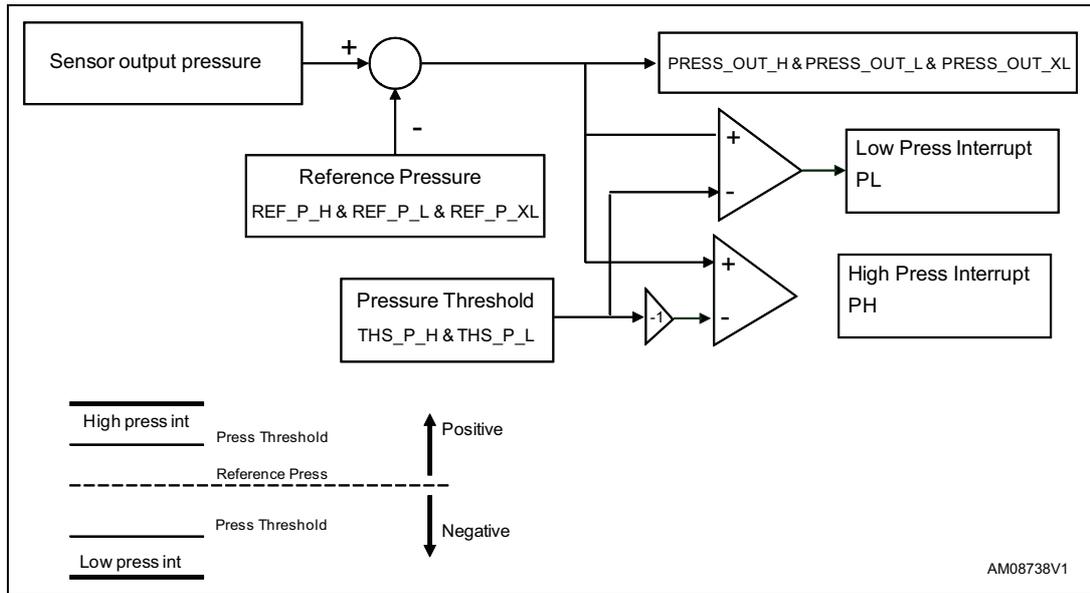
7.9 CTRL_REG4

Interrupt configuration

7	6	5	4	3	2	1	0
0	0	0	0	P1_EMPTY	P1_WTM	P1_Overrun	P1_DRDY

Address: 23h (R/W)

Reset: 00h

Description: INT1 Interrupt pins configuration.

[7:4] Reserved: keep these bits at 0

[3] P1_EMPTY: Empty Signal on INT1 pin

[2] P1_WTM Watermark Signal on INT1 pin

[1] P1_OVERRUN Overrun signal on INT1 pin

[0] P1_DRDY:Data ready signal on INT1 pin

7.10 INTERRUPT_CFG

Interrupt configuration

7	6	5	4	3	2	1	0
RESERVED					LIR	PL_E	PH_E

Address: 24h (R/W)

Reset: 00h

Description: Interrupt differential configuration register. See DIFF_EN bit in CTRL_REG1

[7:3] RESERVED

[2] LIR: Latch Interrupt request into INT_SOURCE register. Default value: 0.
(0: interrupt request not latched; 1: interrupt request latched)

[1] PL_E: Enable interrupt generation on differential pressure low event. Default value: 0.
(0: disable interrupt request;
1: enable interrupt request on measured differential pressure value lower than preset threshold)

[0] PH_E: Enable interrupt generation on differential pressure high event. Default value: 0
(0: disable interrupt request;
1:enable interrupt request on measured differential pressure value higher than preset threshold)

7.11 INT_SOURCE

Interrupt source

7	6	5	4	3	2	1	0
0	0	0	0	0	IA	PL	PH

Address: 25h (R)

Reset: 00h

Description: INT_SOURCE register is cleared by reading it

[7:3] Reserved: keep these bits at 0

[2] IA: Interrupt Active.
(0: no interrupt has been generated; 1: one or more interrupt events have been generated).

[1] PL: Differential pressure Low.
(0: no interrupt has been generated; 1: Low differential pressure event has occurred).

[0] PH: Differential pressure High.
(0: no interrupt has been generated; 1: High differential pressure event has occurred).

7.12 STATUS_REG

Status register

7	6	5	4	3	2	1	0
RES		P_OR	T_OR	RES		P_DA	T_DA

Address: 27h (R)

Reset: 00h

Description: This register is updated every ODR cycle, regardless of BDU value in CTRL_REG1.

P_DA is set to 1 whenever a new pressure sample is available. P_DA is cleared when PRESS_OUT_H (2Ah) register is read.
T_DA is set to 1 whenever a new temperature sample is available. T_DA is cleared when TEMP_OUT_H (2Ch) register is read.
P_OR bit is set to '1' whenever new pressure data is available and P_DA was set in the previous ODR cycle and not cleared. P_OR is cleared when PRESS_OUT_H (2Ah) register is read.
T_OR is set to '1' whenever new temperature data is available and T_DA was set in the previous ODR cycle and not cleared. T_OR is cleared when TEMP_OUT_H (2Ch) register is read.

[7:6] Reserved

[5] P_OR: Pressure data overrun. Default value: 0
(0: no overrun has occurred;
1: new data for pressure has overwritten the previous one)

[4] T_OR: Temperature data overrun. Default value: 0
(0: no overrun has occurred;
1: a new data for temperature has overwritten the previous one)

[3:2] Reserved

[1] P_DA: Pressure data available. Default value: 0
(0: new data for pressure is not yet available;
1: new data for pressure is available)

[0] T_DA: Temperature data available. Default value: 0
(0: new data for temperature is not yet available;
1: new data for temperature is available)

7.13 PRESS_OUT_XL

Pressure data (LSB)

7	6	5	4	3	2	1	0
POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0

Address: 28h (R)

Description: The PRESS_OUT_XL register contains the lowest part of the pressure output value,that is the difference between the measured pressure and the reference pressure (REF_P registers).See AUTOZERO bit in CTRL_REG2.The full reference pressure value is composed by PRESS_OUT_H/_L/_XL and is represented as 2's complement. Pressure Values exceeding the operating pressure Range (see Table 3) are clipped.
Pressure output data: Pout(hPa) = PRESS_OUT / 4096
Example: P_OUT = 0x3ED000 LSB = 4116480 LSB = 4116480/4096 hPa= 1005 hPa
Default Value is 0x2F800 = 760 hPa

[7:0] POUT7 - POUT0: Pressure data LSB

7.14 PRESS_OUT_L

Pressure data (MSB)

15	14	13	12	11	10	9	8
POUT15	POUT14	POUT13	POUT12	POUT11	POUT10	POUT9	POUT8

Address: 29h (R)

Description: The PRESS_OUT_L register contains the middle part of the pressure output value.(See description PRESS_OUT_XL).

[15:8] POUT15 - POUT8: Pressure data

7.15 PRESS_OUT_H

Pressure data (MSB)

24	23	22	21	20	19	18	17
POUT23	POUT22	POUT21	POUT20	POUT19	POUT18	POUT17	POUT16

Address: 2Ah (R)

Description: The PRESS_OUT_H register contains the highest part of the pressure output value.(See description PRESS_OUT_XL).

[24:17] POUT23 - POUT16: Pressure data MSB

7.16 TEMP_OUT_L

Temperature data (LSB)

7	6	5	4	3	2	1	0
TOUT7	TOUT6	TOUT5	TOUT4	TOUT3	TOUT2	TOUT1	TOUT0

Address: 2Bh (R)

Description: The TEMP_OUT_L register contains the low part of the temperature output value.Temperature data are expressed as TEMP_OUT_H & TEMP_OUT_L as 2's complement numbers. Temperature output data:

$T(°C) = 42.5 + (TEMP\_OUT / 480)$

If TEMP_OUT = 0 LSB then Temperature is 42.5 °C

[7:0] TOUT7 - TOUT0: temperature data LSB

7.17 TEMP_OUT_H

Temperature data (MSB)

15	14	13	12	11	10	9	8
TOUT14	TOUT14	TOUT13	TOUT12	TOUT11	TOUT10	TOUT9	TOUT8

Address: 2Ch (R)

Description: The TEMP_OUT_H register contains the high part of the temperature output
                    value.(See description TEMP_OUT_L).

[15:8] TOUT15 - TOUT8: Pressure data

7.18   FIFO_CTRL

FIFO control

7	6	5	4	3	2	1	0
F_MODE2	F_MODE1	F_MODE1	WTM_POINT4	WTM_POINT3	WTM_POINT2	WTM_POINT1	WTM_POINT0

Address: 2Eh (R/W)

Reset: 00h

Description: The FIFO_CTRL registers allows to control the FIFO functionality.

[7:5] F_MODE2-0: FIFO mode selection.See *Table 22*.

[4:0] WTM_POINT4-0 : FIFO threshold.Watermark level setting. See *Table 23*.

Table 20. FIFO mode selection

F_MODE2	F_MODE1	F_MODE0	FIFO mode
0	0	0	BYPASS MODE
0	0	1	FIFO MODE. Stops collecting data when full
0	1	0	STREAM MODE: Keep the newest measurements in the FIFO
0	1	1	STREAM MODE until trigger deasserted, then change to FIFO MODE
1	0	0	BYPASS MODE until trigger deasserted, then change to STREAM MODE
1	0	1	Reserved for future use
1	1	0	FIFO_MEAN MODE: FIFO is used to generate a running average filtered pressure
1	1	1	BYPASS mode until trigger deasserted, then change to FIFO MODE

FIFO_MEAN_MODE: The FIFO can be used for implementing a HW moving average on the
pressure measurements. The number of samples of the moving average can be 2, 4, 8, 16
or 32 samples, by selecting the watermark levels as per *Table 21*.Different configuration are
not guarranted.

Table 21. FIFO watermark selection

WTM_POINT4..0	FIFO_MEAN_MODE Sample Size
00001	2 samples moving average
00011	4 samples moving average
00111	8 samples moving average
01111	16 samples moving average
11111	32 samples moving average

When using the FIFO_MEAN_MODE it is not possible to access the FIFO.

7.19   FIFO_STATUS

FIFO status

7	6	5	4	3	2	1	0
WTM_FIFO	FULL_FIFO	EMPTY_FIFO	DIFF_POINT 4	DIFF_POINT 3	DIFF_POINT 2	DIFF_POINT 1	DIFF_POINT 0

Address: 2Fh (R)

Reset: 00h

Description: FIFO_status

[7] WTM_FIFO: Watermark status
(0: FIFO level lower than watermark level, 1: FIFO is equal or higher than watermark level)

[6] FULL_FIFO: Overrun bit status
(0: FIFO not full,1: FIFO is full)

[5] EMPTY_FIFO: Empty fifo bit
(0: FIFO not empty, 1: FIFO is empty)

[4:0] DIFF_POINT4-0: FIFO stored data level

7.20 THS_P_L

Threshold pressure (LSB)

7	6	5	4	3	2	1	0
THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Address: 30h (R/W)

Reset: 00h

Description: This register contains the low part of threshold value for pressure interrupt generation. The complete threshold value is given by THS_P_H & THS_P_L and is expressed as unsigned number.P_ths (hPa) = (THS_P)/16.

[7:0] THS7-0: LSB Threshold pressure.

7.21 THS_P_H

Threshold pressure (MSB)

15	14	13	12	11	10	9	8
THS15	THS14	THS13	THS12	THS11	THS10	THS9	THS8

Address: 31h (R/W)

Reset: 00h

Description: This register contains the high part of threshold value for pressure interrupt generation.(See description THS_P_L).

[15:8] THS7-0: MSB Threshold pressure.

7.22 RPDS_L

Pressure offset (LSB)

7	6	5	4	3	2	1	0
RPDS7	RPDS6	RSPDS5	RPDS4	RPDS3	RPDS2	RPDS1	RPDS0

Address: 39h (R/W)

Reset: 00h

Description: This register contains the low part of the pressure offset value after soldering,for differential pressure computing. The complete value is given by RPDS_L & RPDS_H and is expressed as signed 2 complement value.

[7:0] RPDS0-7: Pressure Offset for 1 point calibration after soldering

7.23 RPDS_H

Pressure offset (MSB)

15	14	13	12	11	10	9	8
RPDS15	RPDS14	RPDS13	RPDS12	RPDS11	RPDS10	RPDS9	RPDS8

Address: 3Ah (R/W)

Reset: 00h

Description: This register contains the high part of the pressure offset value after soldering (see description RPDS_L)

[15:8] RPDS15-8: Pressure Offset for 1 point calibration after soldering.

8   FIFO operating details

8.1   FIFO registers

This device embeds a 32-slot x 24 bit FIFO pressure data coming from the PRESS_OUT (@ 28..2Ah). It allows lower frequency of serial bus transactions and provides more time to collect all taken measurements. The FIFO can operate in the following modes:

The mode is defined by 3 bits @0x2E: FIFO_CTRL. F_MODE[2:0]

BYPASS MODE [000]

In this mode the FIFO is disabled and stays empty. Pressure is ready directly.

FIFO MODE [001]

All pressure measurement are filling the FIFO. The FIFO content is read by reading the PRESS_OUT registers @28..2Ah). A watermark interrupt can be enabled (CTRL2. WTM_EN) which is raised when the FIFO is filled to the level specified in FIFO_CTRL. WTM_POINT[4:0]. When the FIFO is full, the FIFO stops collecting incoming pressure measurements.

BYPASS TO STREAM MODE [100]

The FIFO is in BYPASS mode till the trigger event. Then the STREAM MODE starts

FIFO MEAN Mode [110] & FIFO_mean_dec = 0

In this mode, the FIFO is used in STREAM mode and its content can be averaged by HW. The hardware calculated running (moving) average can be read in PRESS_OUT registers at anytime. This is used to further reduce the pressure noise at low power.

The number of samples to average is selectable through WTM_POINT[4:0]. See *Table 22*.

Table 22. Running average sample size

WTM_POINT[4:0]	Sample averaged
00001	2
00011	4
00111	8
01111	16
11111	32
others	Reserved

BYPASS to FIFO mode [111]

The FIFO switch from BYPASS to FIFO mode when the event is asserted

Accessing the FIFO data:

FIFO data is read through PRESS_OUT registers. When FIFO is in Stream, Trigger or FIFO mode, a read operation to the PRESS_OUT registers provide the data stored in the FIFO.

Each time data is read from the FIFO, the oldest entry is placed in the PRESS_OUT registers and both single read and burst read operation can be used.

The whole FIFO content can be read by reading 3x32 bytes from PRESS_OUT_XL location in a single I²C read transaction. Internally the reading address will automatically roll back from 0x2A down to 0x28 when FIFO is active to allow a quick read of its content.

9 Hardware digital filter

An embedded digital filter is activated by selecting the FIFO_MEAN_MODE and WTM_POINT (FIFO_CTRL(2Eh)) and activating the FIFO_EN.

The digital filter reduces the pressure noise level to 0.010 hPa rms (1pa at 1 sigma) and allows to reduce the internal ADC HW average reducing the power consumption keeping the same pressure noise level.

Figure 13. Hardware digital filter
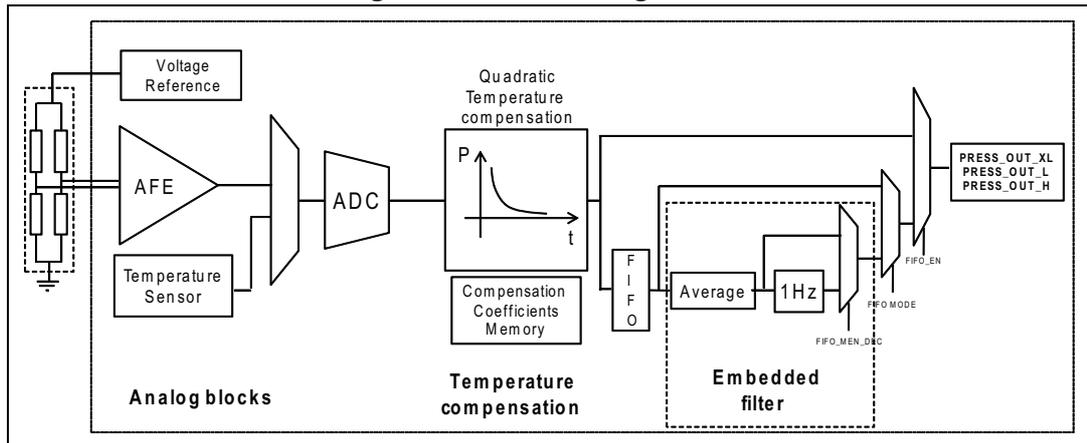
9.1 Filter enabling and suggested configuration

To reduce the internal pressure and temperature average the configuration below can be used:

RES_CONF (10h) = 05h

FIFO_CTRL (2Eh) = C0

CTRL_REG2 (21h) = 40h

In this way, the power consumption at 1 Hz is reduced from 25 μA (typical) to 4.5 μA (typical) with a pressure noise of 0.01 hPa rms

10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 14. Package outline for HCLGA-10L (2.5 x 2.5 x 1.0 mm)
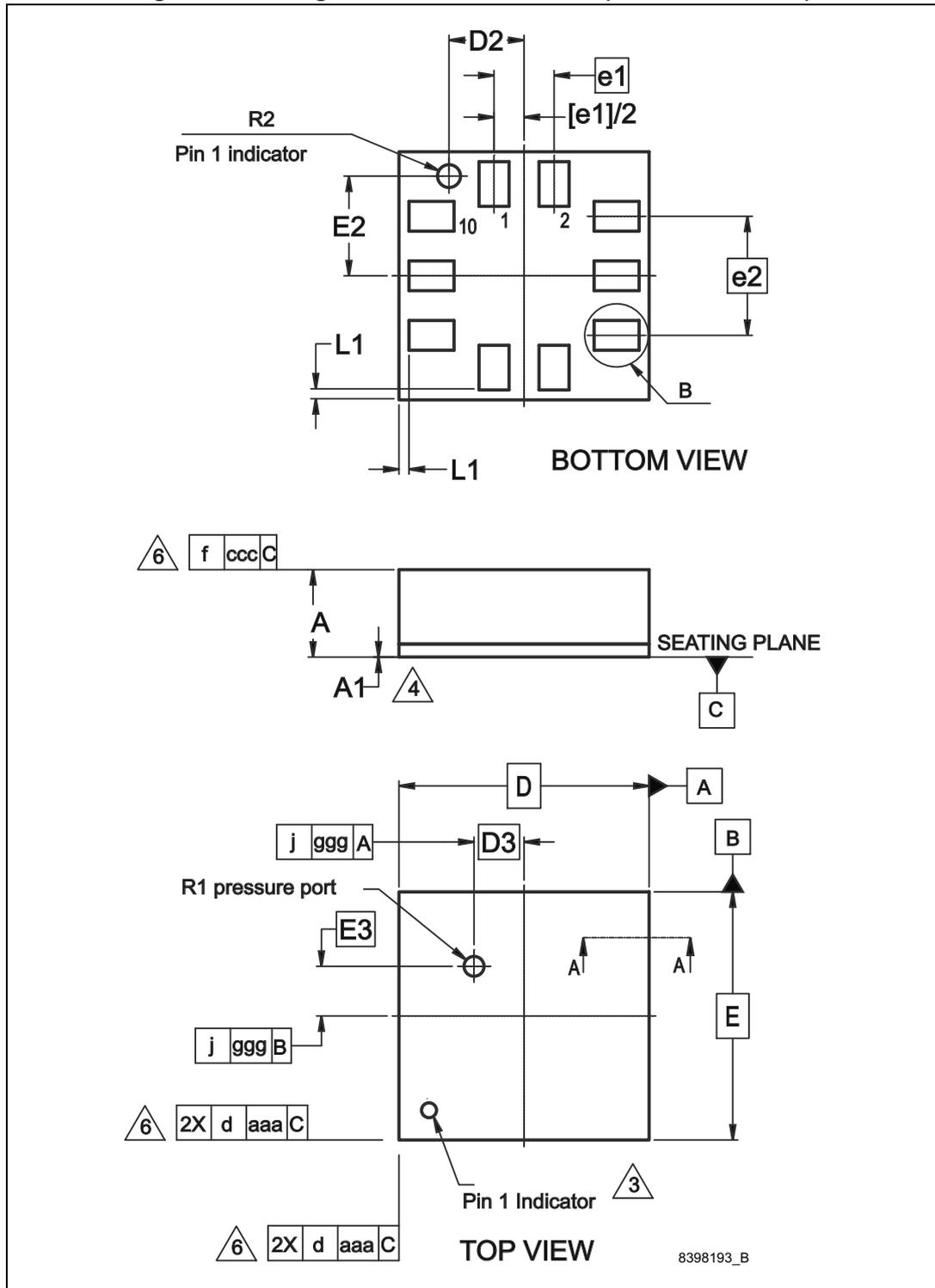
Table 23. HCLGA-10L (2.5 x 2.5 x 1.0 mm) mechanical data

Symbol	Millimeters		
	Min.	**Typ.**	**Max.**
A	0.90	1.00	1.09
A1	0.00	-	0.05
b	0.25	0.30	0.35
D	2.50 BSC		
D2	0.71	0.75	0.79
D3	0.50 BSC		
E	2.50 BSC		
E2	0.97	1.01	1.05
E3	0.50 BSC		
e1	0.60 BSC		
e2	1.20 BSC		
N	10		
L	0.41	0.45	0.49
L1	0.083	0.10	0.17
R1	0.20		
R2	0.15		

11   Revision history

Table 24. Document revision history

Date	Revision	Changes
10-Jul-2013	1	Initial release
15-Jul-2013	2	Modified: THS_P_L and THS_P_H register address *Table 15 on page 21*
14-Jan-2014	3	Added: *Section 2.3: Communication interface characteristics*

Please Read Carefully: